(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 544 229 A1**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **92119988.1**

(22) Date of filing: **24.11.92**

(51) Int. Cl.5: **H01L 27/12**, G02F 1/133

(30) Priority: **25.11.91 JP 334597/91**

(43) Date of publication of application:
02.06.93 Bulletin 93/22

(84) Designated Contracting States:
DE FR GB

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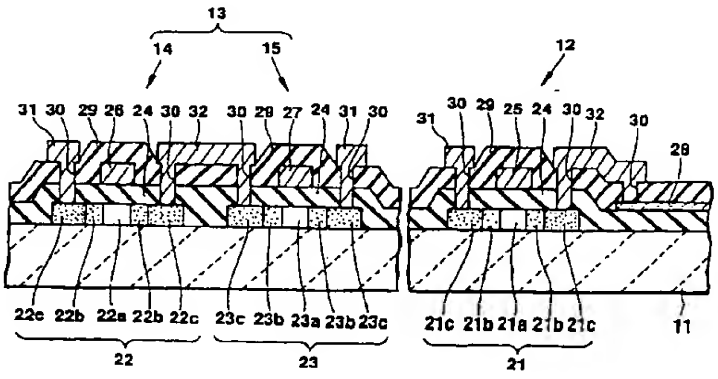
(54) **Thin film transistor device for driving circuit and matrix circuit**

(57) In the case of an LDD-structure thin film transistor, an on-current becomes large as impurity concentration of low level impurity source and drain regions is increased. Then, when the impurity concentration is increased to a first impurity concentration, the on-current reaches to a substantially maximum point. On the other hand, a cut-off current I_{off} becomes substantially minimum when the impurity concentration is decreased to a second impurity concentration. The cut-off current is gradually increased even if the impurity concentration becomes higher or lower than the second impurity concentration. Therefore, impurity concentration of low level impurity source and drain regions (22b) of a thin film transistor (14) for a peripheral circuit is set to a first impurity concentration, and that of low concentration impurity source and drain regions (21b) of a thin film transistor (12) for a matrix circuit is set to a second impurity concentration.

FIG.1



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The present invention relates to a thin film transistor device having a matrix circuit for applying an electric field to a liquid crystal display device and a driving circuit for driving the matrix circuit.

For example, there is used an active matrix type liquid crystal display comprising a matrix circuit for applying an electric field to a liquid crystal display device and a peripheral driving circuit for driving the matrix circuit, each circuit being formed of field effect type thin film transistors.

Fig. 4 shows one example of the circuit structure of such a conventional active matrix type liquid crystal display.

This active matrix type liquid crystal display comprises a matrix circuit 1, one peripheral driving circuit 2 for supplying a scanning signal to an address bus of the matrix circuit 1, and other peripheral driving circuit 3 for supplying a display signal to a data bus of the matrix circuit 1. In the matrix circuit 1, there are formed a large number of scanning electrodes 4 arranged in row and a large number of display electrodes 5 arranged in column, and a thin film transistor 7 for the matrix circuit is formed for each pixel 6 (liquid crystal) corresponding to each cross point of the scanning electrodes 4 and the display electrodes 5. A gate electrode of each thin film transistor 7 is connected to each scanning electrode 4, and a source electrode is connected to the display electrode 5. A drain electrode of each thin film transistor 7 is connected to a pixel capacitive element 8 having a transparent electrode connected to each pixel in parallel. One peripheral circuit 2 comprises a thin film transistor (not shown) for one peripheral circuit, connected to one end of the scanning electrode 4. Other peripheral circuit 3 comprises a thin film transistor for other peripheral circuit, connected to one end of the scanning electrode 5. Then, if the thin film transistor 7 for matrix circuit is turned on, display data is written to the capacitive element 8 in the form of an electric charge. If the thin film transistor 7 for matrix circuit is turned off, the pixel 6 is driven in a predetermined time by the written electric charge.

According to such a conventional thin film transistor device, the thin film transistor 7 forming the matrix circuit 1 and the thin film transistor forming the peripheral driving circuit were formed in the same structure. Therefore, characteristics of the transistor such as a switching speed of the thin film transistor, a cut-off speed or the like were the same in both transistors.

In recent years, display with extremely high precision has been required in the active matrix type liquid crystal display, and it has been needed that the number of thin film transistors, which form the matrix circuit 1 and the peripheral driving circuits 2 and 3, is increased.

However, as the number of the thin film transistors is increased, the consumption current to be consumed in the entire device is increased. In order to this problem, the cut-off current of each thin film transistor 7 must be controlled to be small. On the other hand, the switching speed of each thin film transistor must be increased in accordance with increase in the number of the thin film transistors. However, as is well-known, the on-current must be increased in order to increase the switching speed, and the cut-off current is also increased by the increase in the on-current. For this reason, the above two requirements cannot be satisfied.

An object of the present invention is to provide a thin film transistor device wherein the number of thin film transistors, which forms a matrix circuit and peripheral driving circuits, can be considerably increased, an on-current can be increased, and a cut-off current can be reduced.

The thin film transistor device of the present invention comprises a first thin film transistor including a semiconductor layer having a channel region, source and drain regions, coupled to ends of the channel region and having low level impurity region and high level impurity region, a gate insulating film, a gate electrode, and source and drain electrodes; and a second thin film transistor having a semiconductor layer including a channel region, source and drain regions coupled to ends of the channel region and having a low level impurity region and a high level impurity regions, a gate insulating film, a gate electrode, and source and drain electrodes, impurities existing in the first thin film transistor and those in the second thin film transistor being of the same conductive type, and concentration of the low impurity level regions of the first thin film transistor set to be higher than that of the low level impurity regions of the second thin film transistor.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is an enlarged cross sectional view showing one embodiment of a thin film transistor device according to the present invention;

Fig. 2 is a flow chart showing the processes of manufacturing the thin film transistor device of Fig. 1;

Fig. 3 is a view showing the relationship between concentration of low level impurity regions and a drain current according to the thin film transistor structured as shown in Fig. 1; and

Fig. 4 is a plane view showing a conventional active matrix type crystal liquid display.

Fig. 1 shows a thin film transistor device according to the present invention.

In the thin film transistor device, a thin film transistor 12 for a matrix circuit, which is formed of an NMOS thin film transistor, and a thin film transistor 13 for a peripheral circuit, which is formed of a CMOS thin film transistor, are formed on each predetermined portion of the upper surface of a transparent substrate 11 formed of glass or the like. The thin film transistor 13 for a peripheral circuit, which is formed of the CMOS thin film transistor, comprises an NMOS thin film transistor 14 and a PMOS thin film transistor 15.

The thin film transistors 12, 14, and 15 comprise semiconductor thin films which are patterned on each predetermined portion of the upper surface of the transparent substrate 11. The thin film transistors 12, 14, and 15 are LDD(Lightly Doped Drain) structured. In details, the central portions of the semiconductor thin films 21, 22, 23 of the thin film transistors 12, 14, 15 are used as channel regions 21a, 22a, and 23a, respectively, and both sides of the channel regions 21a, 22a, 23a are used as source and drain regions 21b, 22b, 23b, which are formed of low impurity concentration regions. Moreover, both sides of the source and drain regions 21b, 22b, 23b are used as source and drain regions 21c, 22c, 23c, which are formed of high level impurity regions. A gate insulating film 24 is formed on the entire surface of the semiconductor thin films 21, 22, 23, and the transparent substrate 11. Gate electrodes 25 to 27 are formed on the respective portions of the upper surface of the gate insulating film 24 each corresponding to the channel regions 21a, 22a, 23a. A transparent capacitive electrode 28, which is formed of ITO (Indium Tin Oxide), is formed on a predetermined portion of the upper surface of the gate insulating film 24. A passivating insulating films 29 is formed on the entire surface of the gate insulating films 24, the gate electrodes 25 to 27, and the transparent capacitive electrode 28. Contact holes 30 are formed at the portions of the passivating film 29 and the gate insulating film 24 which correspond to the high level impurity source and drain regions 21c, 22c and 23c. Source and drain electrodes 31 are formed in the contact holes 30 and on predetermined portions of the upper surface of the passivating film 29. In this case, one of source and drain electrodes 31 of the thin film transistor 12 for the matrix circuit is connected to one end portion of the transparent capacitive electrode 28. Moreover, one of source and drain regions 22c of NMOS thin film transistor 14 and one of source and drain regions 23c of PMOS thin film transistor 15 are electrically connected to each other through a drain electrode 32 such that one CMOS thin film transistor is formed by a pair of thin film transistors 14 and 15.

For the above structured thin film transistor device, note that impurity concentration of the low level impurity source and drain regions 22b of the NMOS transistor 14, which forms the thin film transistor 13 for the peripheral circuit, is higher than of the low level impurity source and drain regions 21b of the thin film transistor 12 for the matrix circuit.

A method for manufacturing the thin film transistor device will be explained with reference to Fig. 2 showing the processes of manufacturing the thin film transistor device.

First, in a semiconductor thin film deposition process 41, an amorphous silicon film for forming semiconductor thin films 21 to 23 is deposited to have a thickness of about 500Å on the entire surface of the transparent substrate 11 by plasma CVD. In an ion implantation process 42, an oxide film serving as a protection film for ion-implantation is deposited to have a thickness of about 1400Å on the entire upper surface of the amorphous silicon film by a sputtering device. Thereafter, photoresist is used as a mask, and impurities are implanted five times in the following manner by an ion-implantation device.

At the first ion implantation, a phosphorus ion is implanted in the portions of the amorphous silicon film where the low level impurity source and drain regions 21b of the thin film transistor 12 for the matrix circuit are to be formed, under the conditions of accerlation energy of 130 keV and a dose of 1×10^{13} atom/cm^2.

At the second ion implantation, a phosphorus ion is implanted in the portions of the amorphous silicon film where the low level impurity source and drain regions 22b of the NMOS thin film transistor 14 as an element of the thin film transistor 13 for the peripheral circuit are to be formed, under the conditions of accerlation energy of 130 keV and a dose of 5×10^{13} atom/cm^2.

At the third ion implantation, a boron ion is implanted in the portions of the amorphous silicon film where the low level impurity source and drain regions 23b of the PMOS thin film transistor 15 as an element of the thin film transistor 13 for the peripheral circuit are to be formed, under the conditions of accerlation energy of 40 keV and a dose of 5×10^{13} atom/cm^2.

At the fourth ion implantation, a phosphorus ion is implanted in the portions of the amorphous silicon film where the high level impurity source and drain regions 22c of the NMOS thin film transistor 14 for the peripheral circuit are to be formed, under the conditions of accerlation energy of 130 keV and a dose of 3×10^{15} atom/cm^2.

At the fifth ion implantation, a boron ion is implanted in the portions of the amorphous silicon film where the high level impurity source and drain

regions 23c of the PMOS thin film transistor 15 for the peripheral circuit are to be formed, under the conditions of accerlation energy of 40 keV and a dose of 1×10^{15} atom/cm^2.

Thereafter, an oxide film serving as a protection film for ion implantation is etched.

In an annealing process 43, an XeCl eximer laser is irradiated on the amorphous silicon film. Thereby, the amorphous silicon film is crystallized into a polysilicon film, and the implanted impurities are activated. In an isolation process 44, an unnecessary portion of the polysilicon film is etched, so that each of semiconductor thin films 21, 22, 23 is shaped in an island on each predetermined portion of the upper surface of the transparent substrate 11. As already explained, since impurities are implanted in the silicon films and activated, the central portions of the semiconductor thin films 21, 22, 23 which remains the intrinsic semiconductor, are used as channel regions 21a, 22a, and 23a, respectively. Both sides of the channel regions 21a, 22a, 23a are used as low impurity diffusion regions. Moreover the outer side of each of low impurity diffusion regions are used as high impurity diffusion regions.

In a gate insulating film deposition process 45, the gate insulating film 24, which is formed of silicon oxide or silicon nitride, is deposited to have a thickness of about 1000 to 1500Å on the entire surfaces of the substrate 11 and the semiconductor films 21 to 23 by sputtering or plasma CVD. In a gate electrode deposition process 46, gate electrodes 25 to 27, which are formed of aluminum chrome or the like, are formed by patterning to have a thickness of about 1000Å on the upper surface of the gate insulating film 24, each corresponding to the channel regions 21a, 22a, 23a, by a sputtering device. In a transparent electrode deposition process 47, the transparent capacitive electrode 28, which is formed of ITO, is formed and patterned on a predetermined portion of the upper surface of the gate insulating film 24 to have a thickness of about 500Å. In a passivating film deposition process 48, the layer insulating film 29, which is formed of silicon nitride, is deposited to have a thickness of about 3000Å on the entire surfaces of the gate insulating film 24 and the gate electrodes 25 to 27, and the transparent electrode 28, by plasma CVD. In source and drain electrodes deposition process 49, the contact holes 30 are formed at the portions of the passivating film 29 and the gate insulating film 24 which correspond to high level impurity source and drain regions 21c, 22c, 23c, and one end the transparent electrode 28. Thereafter, the source and drain electrodes 31, which are formed of aluminum, are formed to have a thickness of about 5000Å, in the contact holes 30 and on predetermined portions of the upper surface of the layer insulating film 29 by the sputtering device. In this way, the matrix circuit driving device is manufactured.

Fig. 3 is a view showing the relationship between impurity concentration of the source and drain regions existing low level impurities according to the thin film transistors 12 and 14 and a drain current. As is obvious from the figure, an on-current I_{on} becomes larger as impurity concentration is higher, and at the impurity concentration Y, the on-current I_{on} reaches to a substantially maximum point. On the other hand, the cut-off current I_{off} becomes substantially minimum at the impurity concentration X (X < Y), and gradually increased even if the impurity concentration becomes larger or smaller than impurity concentration X.

According to the thin film transistor device as described above at the first ion implantation, the phosphorus ion is implanted in the low level impurity source and drain regions 21b of the thin film transistor 12 under the conditions of accerlation energy of 130 keV and a dose of 1×10^{13} atom/cm^2. Then, at the second ion-implantation, the phosphorus ion is implanted in the low level impurity source and drain regions 22b of the NMOS thin film transistor 14 under the conditions of accerlation energy of 130 keV and a dose of 5×10^{13} atom/cm^2. Therefore, the impurity concentration of the source and drain regions 22b of the thin film transistor 14 is higher than that of the source and drain regions 21b of the the thin film transistor 12. The impurity concentration of the source and drain regions 22b of the thin film transistor 14 is substantially maximum point Y of the on-current I_{on}. The impurity concentration of the source and drain regions 21b of the thin film transistor 12 is substantially minimum point X of the cut-off current I_{off}. Therefore, in the NMOS thin film transistor 14, constituting the thin film transistor 13 for the peripheral circuit, the on-current is set to maximum, that is, the switching speed is set to maximum. Also, in the thin film transistor 12 for the matrix circuit, the cut-off current is set to minimum.

According to the above embodiment, the semiconductor thin films 21, 22, 23 were directly formed on the upper surface of the transparent substrate 11. However, the present invention is not limited to the above embodiment. More specifically, a ground layer, which is formed of silicon oxide or silicon nitride, is formed on the upper surface of the transparent substrate 11, and the semiconductor thin films 21, 22, 23 may be formed on the upper surface of the ground layer. The peripheral circuit 13 may be formed on a substrate different from the substrate on which the matrix circuit 12 is formed. The peripheral circuit 13 may be formed of either the NMOS thin film transistor 14 or the PMOS thin film transistors. In the above

embodiment, the PMOS thin film transistor was formed in only the peripheral circuit, and not formed in the matrix circuit. Due to this, the impurity concentration was determined so as to satisfy the performance which is required in the peripheral circuit. In the case where the PMOS thin film is formed in the matrix circuit, the impurity concentration of the low level impurity source and drain regions for the peripheral circuit may be higher than that of the matrix circuit. The above embodiment explained the case that the low level impurity regions are formed in the source regions. However, the low level impurity regions may be not formed in the source region. Moreover, the present invention can be widely applied to a thin film transistor memory, an image sensor or the like other than the liquid crystal display.

According to the present invention, the impurity concentration of the low level impurity region of the thin film transistor formed in the peripheral circuit is higher than that of the low level impurity region of the thin film transistor formed in the matrix circuit. Therefore, the on-current can be sufficiently enhanced and the cut-off current can be sufficiently lowered. In addition, the switching speed can be higher, and a display quality can be improved.

Claims

1. A thin film transistor device comprising:

a first thin film transistor (14) including a semiconductor layer (22) having a channel region (22a), and source and drain regions coupled to ends of the channel region (22a), and having a low level impurity region (22b) and a high level impurity region (22c), a gate insulating film (24), a gate electrode (26), and source and drain electrodes (31, 32); and

a second thin film transistor (12) including a semiconductor layer (21) having a channel region (21a) and, source and drain regions coupled to ends of the channel region (21a), and having a low level impurity region (21b) and a high level impurity region (21c), a gate insulating film (24) a gate electrode (25), and source and drain electrodes (31, 32),

characterized in that

the impurities existing in said first thin film transistor (14) and those in said second thin film transistor (12) have the same conductive type, and the concentration of said low level impurity region (22b) of said first thin film transistor (14) is set to be higher than that of said low level impurity region (21b) of said second thin film transistor (12).

2. The thin film transistor device according to claim 1, characterized in that said first and second thin film transistors (14, 12) are N-MOS field effect type thin film transistors.

3. The thin film transistor device according to claim 1 or 2, characterized in that the impurity concentration of said low level impurity regions (22b) of said first thin film transistor (14) is several times as high as that of said low level impurity regions (21b) of said second thin film transistor (12).

4. The thin film transistor device according to claim 1, 2 or 3, characterized in that the impurity concentration of said low level impurity regions (22b) of said first thin film transistor (14) is selected to correspond to substantially a maximum point of an on-current

5. The thin film transistor device according to any one of preceding claims, characterized in that the impurity concentration of said low level impurity regions (21b) of said second first thin film transistor (12) is selected to correspond to substantially a minimum point of a cut-off current.

6. The thin film transistor device according to claim 1, characterized in that including an insulating substrate (11) on which a plurality of second thin film transistors (12) are formed in matrix to constitute a matrix circuit section (1).

7. The thin film transistor device according to claim 6, characterized in that a plurality of said first thin film transistors (12, 14) are formed on the outer periphery of said matrix circuit section (1) to constitute driving circuit sections (2, 3) for driving said second thin film transistors.

8. A thin film transistor device comprising:

a transparent substrate (11);

a matrix circuit section (1) including second field effect type thin film transistors (12) formed on said transparent substrate (11) in matrix, each comprising a semiconductor layer (21) having a drain region having a low level impurity region (21b) and a high level impurity region (21c); and

a driving circuit section (2, 3) including a plurality of first field effect type thin film transistors (14) formed on said transparent substrate (11) in matrix, on the outer periphery of said matrix circuit section, each having the same channel type as each of said second thin film transistors (12) and comprising a semiconductor layer (22) including a drain region having a low level impurity region (22b) and a high level impurity region (22c),

characterized in that

the impurity concentration of said low level impurity region (22b) of each of said first thin film transistors (14) is higher than that of low level impurity region (21b) of each of said second thin film transistors (12).

9. The thin film transistor device according to claim 8, characterized by comprising pixel electrodes (28) for applying electrical field to a liquid crystal, to each of which each of said second thin film transistors is connected.

10. The thin film transistor device according to claim 9, characterized in that said first and second thin film transistors (12, 14) are NMOS field effect type thin film transistors.

11. The thin film transistor device according to claim 9, characterized in that the impurity concentration of said low level impurity region (22b) of each of said first thin film transistors (14) is several times as large as that of each of said low level impurity regions (21b) of said second thin film transistors (12).

12. The thin film transistor device according to claim 9, characterized in that the impurity concentration of said low level impurity region (22b) of each of said first thin film transistors (14) is selected to correspond to substantially a maximum point of an on-current.

13. The thin film transistor device according to claim 9, characterized in that the impurity concentration of said low level impurity region (22b) of each of said second thin film transistors (12) is selected to correspond to substantially a minimum point of a cut-off current.

FIG.1

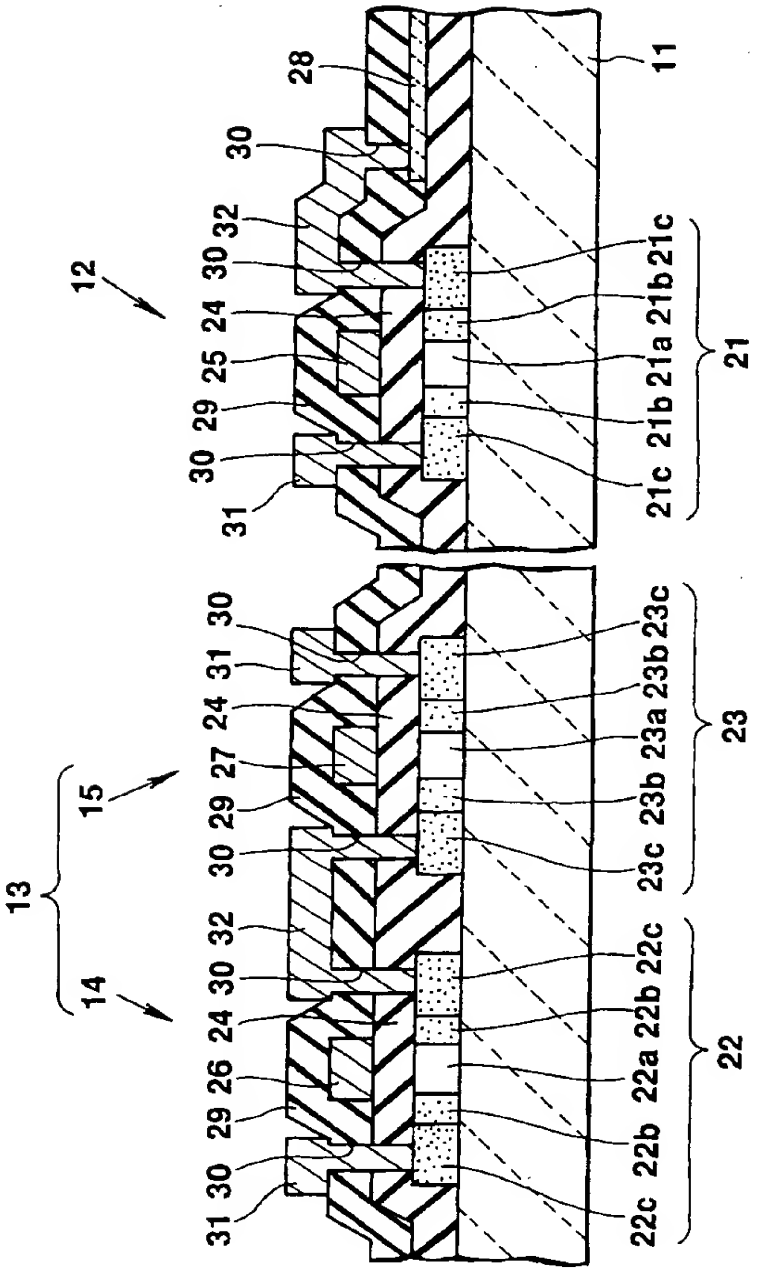
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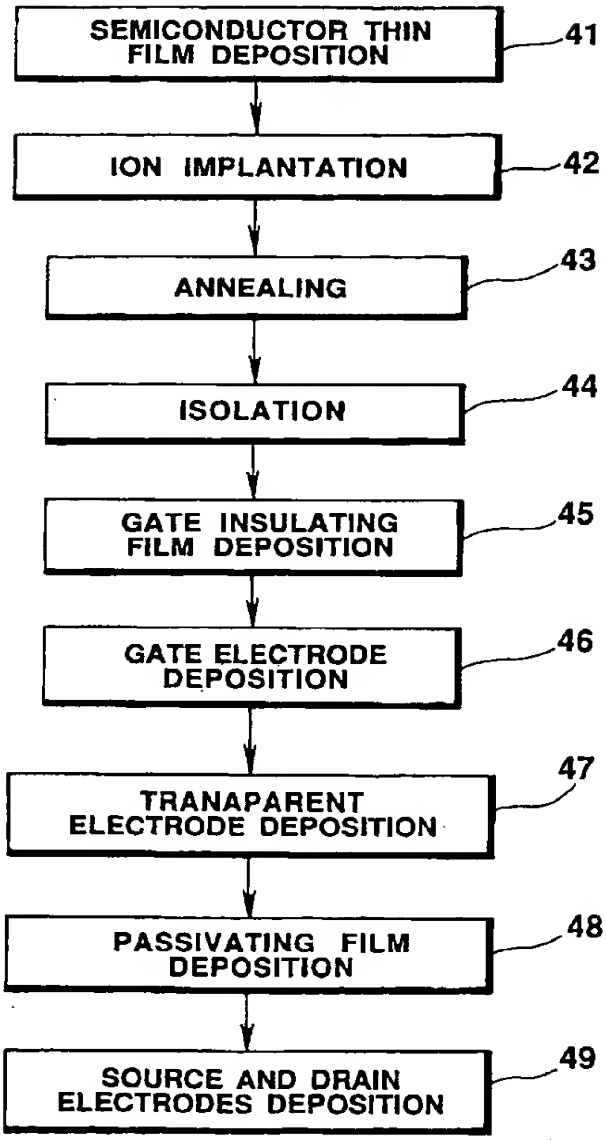
FIG.2


SEMICONDUCTOR THIN FILM DEPOSITION
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ANNEALING
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ISOLATION
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GATE INSULATING FILM DEPOSITION
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GATE ELECTRODE DEPOSITION
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TRANAPARENT ELECTRODE DEPOSITION
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PASSIVATING FILM DEPOSITION
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SOURCE AND DRAIN ELECTRODES DEPOSITION
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FIG. 3

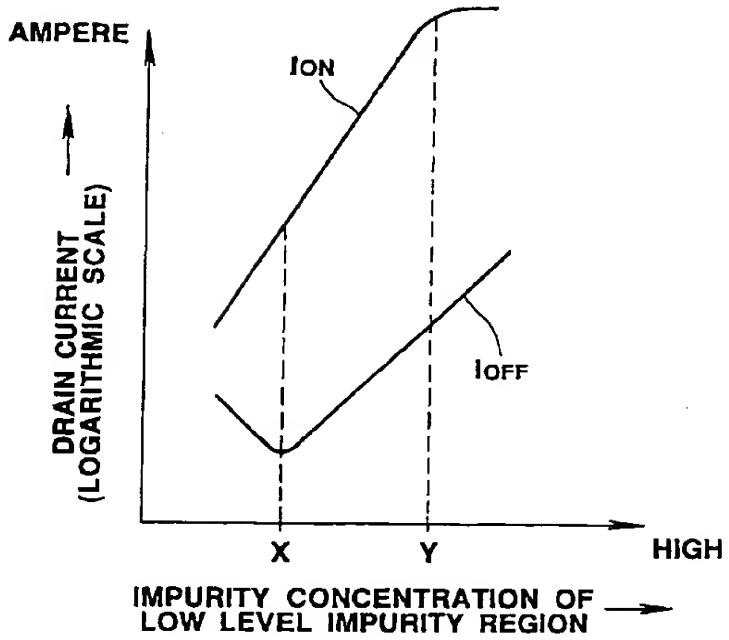
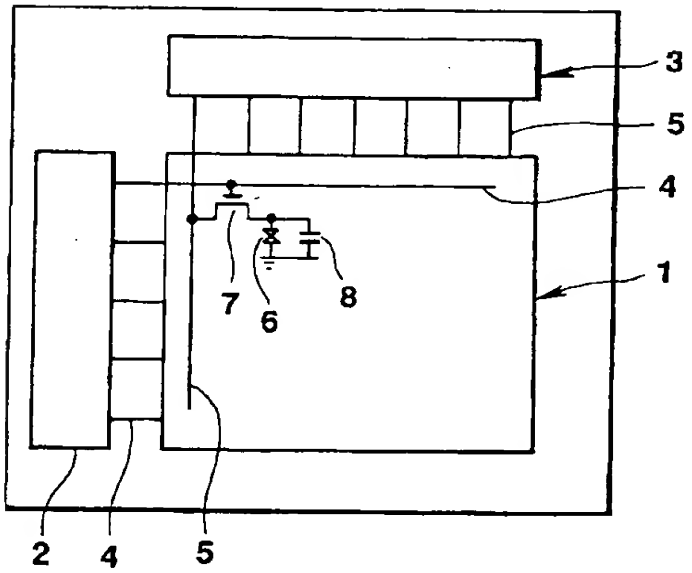


FIG. 4
(PRIOR ART)



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EUROPEAN SEARCH REPORT

Application Number
EP 92 11 9988

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 356 039 (SEIKO EPSON CORPORATION) 28 February 1990	1-2,8-10	H01L27/12 G02F1/133
A	* page 3, column 3, line 57 - page 3, column 4, line 34; claims 1,4-5,7-9; figure 3 *	3,11	
Y	PATENT ABSTRACTS OF JAPAN vol. 7, no. 258 (E-211)(1403) 17 November 1983 & JP-A-58 142 566 (SUWA SEIKOSHA K.K.) 24 August 1983 * abstract *	1-2,8-10	
A	EP-A-0 342 925 (SEIKO EPSON CORPORATION) 23 November 1989 * page 6, line 44 - page 8, line 6 * * page 12, line 17 - page 12, line 30; claims 1-4,8; figures 1,4-7 *	1,8	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H01L
G02F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 FEBRUARY 1993	FRANSEN L.J.L.

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